14 Semiconductor Electronics: Materials, Devices and Simple Circuits

MULTIPLE CHOICE QUESTIONS—I

Q14.1. The conductivity of a semiconductor increases with increase in temperature, because

(*a*) number density of free current carriers increases.

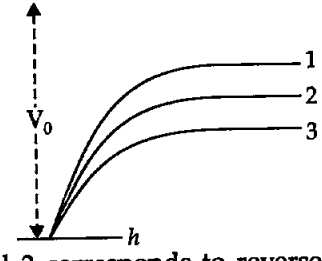
(*b*) relaxation time increases.

(*c*) both number density of free current carriers and relaxation time increases.

(*d*) number density of current carriers increases and relaxation time decreases, but effect of decrease in relaxation time is much less than increase in number density.

Ans. (*d*): In semiconductor, the density of charge carriers(electron, holes) are very small, so its resistance is high. When temperature increases the charge carriers (density) increases which increases the conductivity. As temperature of semiconductor increases, the speed of free electrons increases which decrease the relaxation time. As the density of charge carrier is small so there is small effect on decrease of relaxation time.

Q14.2. In given figure, V_0 is the potential barrier across a p-n junction, when no battery is connected across the junction



(*a*) 1 and 3 both corresponds to forward bias of junction.

(*b*) 3 corresponds to forward bias of junction and 1 corresponds to reverse bias of junction.

(*c*) 1 corresponds to forward bias and 3 corresponds to reverse bias of junction.

(*d*) 3 and 1 both corresponds to reverse bias of junction.

Main concept used: Thickness of depletion layer in p-n junction.

Ans. (*b*): When p-n junction is in forward bias, it compresses or decreases the depletion layer so potential barrier in forward bias decreases and in reverse bias potential barrier increases.

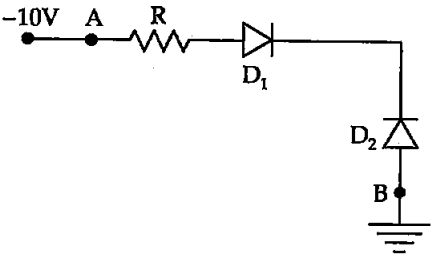
Q14.3. In given figure below, assuming the diodes to be ideal,

(*a*) D_1 is forward biased and D_2 in reverse biased and hence current flows from A to B.

(*b*) D_2 is forward biased and D_1 is reverse biased and hence no current flows from B to A and vice versa.

(*c*) D_1 and D_2 both are forward biased and hence current flows from A to B.

(*d*) D_1 and D_2 are both in reverse bias hence no current flows from A to B and vice-versa.



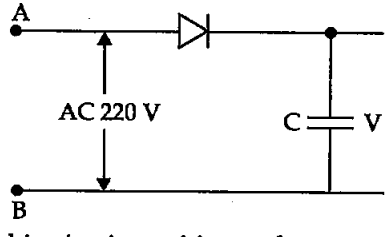
Main concept used: Potential at the ends of diode.

Ans. (*b*): In circuit, A is at –10V and B is at 0V. So B is positive than A. So D_2 is in forward bias and D1 is in reverse bias so no current flows from A to B or B to A.

Q14.4. A 220 V AC supply is connected between points A and B (figure). What will be the potential difference V across the capacitor?

(*a*) 220 V (*b*) 110 V

(*c*) 0V (*d*) $220\sqrt{2}$ V



Main concept used: p-n junction conducts current in forward bias *i.e.*, in positive cycle.

Ans. (*d*): Potential difference across capacitor will be peak voltage when diode is in forward bias. Diode will be in forward bias when end A is at positive potential of cycle. So potential at C = peak value of $V = V_{rms}\sqrt{2} = 220\sqrt{2}$ V.

Q14.5. Hole in semiconductor is

(*a*) an antiparticle of electron.

(*b*) a vacancy created when an electron leaves a covalent bond.

(*c*) absence of free electrons.

(*d*) an artificially created particle.

Ans. (*b*): Atoms of semiconductor are binded by covalent bonds between the atoms of same or different type. Due to thermal agitation when an electron leaves its position and become free, then it leaves a vacancy of electron, this vacancy in the bond (covalent) is called hole.

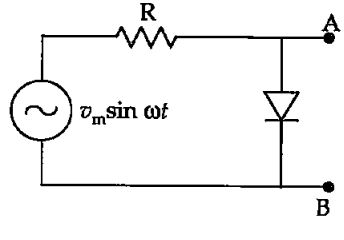
Q14.6. The output of the given circuit in figure

(*a*) would be zero at all times.

(*b*) would be like a half wave rectifier with positive cycles in output.

(*c*) would be like a half wave rectifier with negative cycles in output.

(*d*) would be like that of a full wave rectifier.



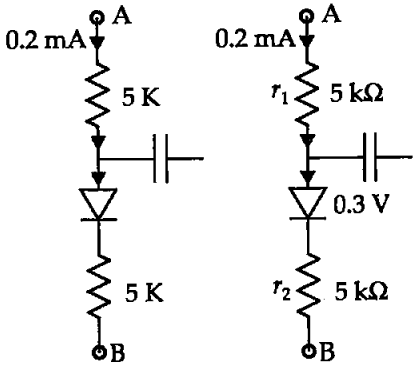
Ans. (*c*): When positive cycle is at A, diode will be in forward bias and resistance due to diode is approximately zero so potential across diode will be about zero.

Similarly, when there is negative half cycle at A, diode will be in reverse bias and resistance will be maximum so potential difference across diode is $V_m \sin \omega t$ with negative at A.

So we get only negative output at A so it behaves like a half wave rectifier with negative cycle at A in output, verifies the answer (*c*).

Q14.7. In the circuit shown in figure below, if the diode forward voltage drop is 0.3V, the voltage difference between A and B is

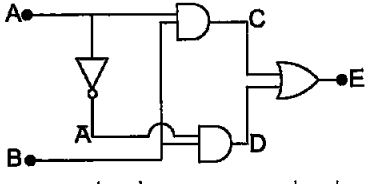
(*a*) 1.3 V (*b*) 2.3 V
(*c*) 0 V (*d*) 0.5 V



Ans. (*b*): In the middle right of the circuit the capacitor behaves like an open circuit for d.c 0.2 mA current so current will flow from A to B only. Let potential across A and B is V, so by Kirchhoff's loop law

$$V_{AB} = (5000 \times 0.2 \times 10^{-3}) + 0.3 + 5000 \times 0.2 \times 10^{-3}$$
$$V_{AB} = 1\text{ V} + 0.3\text{ V} + 1\text{ V}$$
$$V_{AB} = 2.3\text{ Volt}$$

Q14.8. Truth table for the given circuit (Figure) is



(*a*)

A	B	E
0	0	1
0	1	0
1	0	1
1	1	0

(*b*)

A	B	E
0	0	1
0	1	0
1	0	0
1	1	1

(*c*)

A	B	E
0	0	0
0	1	1
1	0	0
1	1	1

(*d*)

A	B	E
0	0	0
0	1	1
1	0	1
1	1	0

Ans. (*c*)

A	B	$\bar{A}$	C	D	E
0	0	1	0	0	0
0	1	1	0	1	1
1	0	0	0	0	0
1	1	0	1	0	1

MULTIPLE CHOICE QUESTIONS—II MORE THAN ONE OPTION

Q14.9. When an electric field is applied across a semiconductor.

(*a*) electrons move from lower energy level to higher energy level in the conduction band.

(*b*) electrons move from higher energy level to lower energy level in the conduction band.

(*c*) holes in the valence band move from higher energy level to lower energy level.

(*d*) holes in the valence band move from lower energy level to higher energy level.

Main concept used: Motion of a charged particle in electric field.

Ans. (*a*) and (*c*): In the direction of electric field the P.E. or energy of electric field decreases. So electrons always move opposite to direction of E.F., *i.e.* from lower energy level to higher energy level and holes move from higher energy level to lower energy level.

In semiconductors, electrons are in conduction band and holes are in valence band.

Q14.10. Consider an *n-p-n* transistor with its base-emitter junction forward biased and collector-base junction reversed biased. Which of the following statements are true?

(*a*) Electrons crossover from emitter to collector.

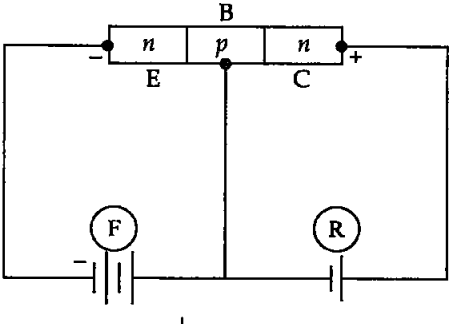
(*b*) Holes move from base to collector.

(*c*) Electrons move from emitter to base.

(*d*) Electrons from emitter move out of base without going to collector.

Main concept used: Working of transistor

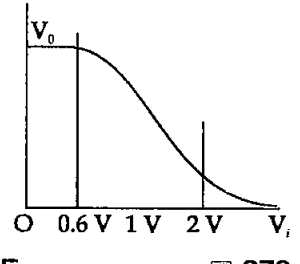
Ans. (*a*) and (*c*): Electrons are repelled by forward bias from emitter to collector ≅ 5% of electrons combine with holes of base and rest 95% electrons of emitter are attracted by reverse bias of collector-base junction.



So electrons move from emitter to collector through base *i.e.*, emitter to base verifies (a) and (c).

Q14.11. Figure given alongside shows the transfer characteristics of a base biased CE transistor. Which of the following statements are true?

(*a*) At V_i = 0.4 V, transistor is in active state.



(*b*) At $V_i = 1$ V, it can be used as an amplifier.
(*c*) At $V_i = 0.5$ V, it can be used as a switch turned off.
(*d*) At $V_i = 2.5$ V, it can be used as a switch turned on.

Ans. (*a*) At $V_i = 0.4$ V there is no collector current only output voltage is V_0 due to V_{ce} battery. So at 0.4 V transistor is not in active mode.
(*b*) When at $V_i = 1$ volt, transistor is between active region (0.6 V to 2 V). So it can be used as an amplifier.
(*c*) At $V_i = 0.5$ V, the transistor is in cut-off state and it can be used as a switch turned off.
(*d*) At $V_i = 2.5$ V, the transistor is beyond active region. The collector current is in saturated state and there is no effect on changing input voltage and the transistor can be used as a switch turned on.
So, the statements (*b*), (*c*) and (*d*) are true.

Q14.12. In a *n-p-n* transistor circuit, the collector current is 10 mA. If 95% of the electrons emitted (by emitter) reach the collector, which of the following statements are true?
(*a*) The emitter current will be 8 mA.
(*b*) The emitter current will be 10.53 mA.
(*c*) The base current will be 0.53 mA.
(*d*) The base current will be 2 mA.

Ans. (*b*) and (*c*): $I_c = 10$ mA

$$I_c = 95\% \text{ of } I_e \quad \text{or} \quad I_c = \frac{95}{100} I_e$$

$$I_e = \frac{10 \text{ mA} \times 100}{95} = 10.53 \text{ mA}$$

$$I_b + I_c = I_e$$

So $$I_b = I_e - I_c = 10.53 - 10 = 0.53 \text{ mA}$$

Q14.13. In the depletion region of a diode
(*a*) there are no mobile charges.
(*b*) equal number of holes and electrons exist, making the region neutral.
(*c*) the recombination of holes and electrons has taken place.
(*d*) immobile charged ions exist.

Ans. (*a*), (*b*), (*c*) and (*d*): During formation of *p-n* junction electrons from *n* side and holes from *p* side move towards each other and form a potential barrier across the junction. Within the barrier there are holes and electrons or ions which cannot move.

So in depletion layer no mobile charges but there are negative and positive ions; barrier layer was formed by recombination of electrons and holes when *pn* junction formed.

Q14.14. What happens during the regulation action of a Zener diode?

(*a*) The current and voltage across the Zener diode remains fixed.

(*b*) The current through the series resistance (R_S) changes.

(*c*) The Zener resistance is constant.

(*d*) The resistance offered by the Zener diode changes.

Ans. (*b*) and (*d*): During action of regulation, current in R_s changes and resistance offered by Zener diode changes. The current through the Zener diode changes but voltage across the Zener remains constant.

Q14.15. To reduce the ripples in a rectifier circuit with capacitor filter

(*a*) R_L should be increased.

(*b*) input frequency should be decreased.

(*c*) input frequency should be increased.

(*d*) capacitors with high capacitance should be used.

Main Concept: The Ripple factor (r) of full-wave rectifier is given by $r = \dfrac{1}{4\sqrt{3} \cdot R_L C_V}$ or $r \propto \dfrac{1}{R_L} \Rightarrow r \propto \dfrac{1}{C}$ and $r \propto \dfrac{1}{V}$

Ans. (*a*), (*c*) and (*d*): As the ripple factor

$$r = \frac{1}{4\sqrt{3}R_L C_V}$$

So to decrease r, R_L and C must be increased.

Input frequency should be increased.

Q14.16. The breakdown in a reverse biased *p-n* junction diode is more likely to occur due to

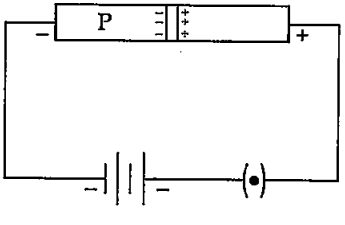
(*a*) large velocity of the minority charge carriers if the dopping concentration is small.

(*b*) large velocity of the minority charge carriers if the dopping concentration is large.

(*c*) strong electric field in a depletion region if the dopping concentration is small.

(*d*) strong electric field in a depletion region if the dopping concentration is large.

Ans. (*a*) and (*d*): In reverse biasing, minority charge carriers accelerate due to high electric field applied (due to reverse P.D.). So the minority charge carrier in both junction accelerated toward depletion layer, which on striking with atoms causes ionisation of atoms resulting the secondary electron and so more number of charge carriers constitute more current in reverse direction.



More current in thin depletion layer is due to the heavy dopping and large no. of ions in the depletion layer which give rise to strong electric field across the junction.

VERY SHORT ANSWER TYPE QUESTIONS

Q14.17. Why are elemental dopants for silicon or Germanium usually chosen from group XIII or XV?

Ans. The size of the dopant atom should be equivalent to the size of Si or Ge. So that the symmetry of pure Si or Ge, does not disturb and dopants can contribute the charge carrier on forming covalent bonds with Si or Germanium atoms. As the silicon and germanium belongs to XIV th group so similar size of atom will be in XIII and XV grp of modern periodic table.

Q14.18. Sn, C, Si, Ge are all group XIV elements. Yet, Sn is a conductor, C is an insulator, while Si and Ge are semiconductors. Why?

Main concept used: Conduction level of an element depends on the energy gap between valence and conduction band of element.

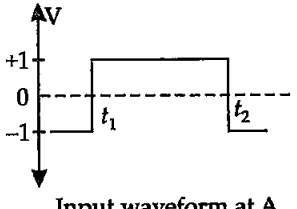
Ans. A material will conduct current if there is no energy gap between conduction and valence band in energy band diagram of atom. This energy gap decreases from insulator to semiconductor and from semiconductor to conductor.

The energy gaps in Sn, C, Si and Ge are 0 eV, 0.54 eV, 1.1 eV and 0.7 eV respectively related to their atomic size. So the Sn is a conductor, C is an insulator while Si and Ge are semiconductors.

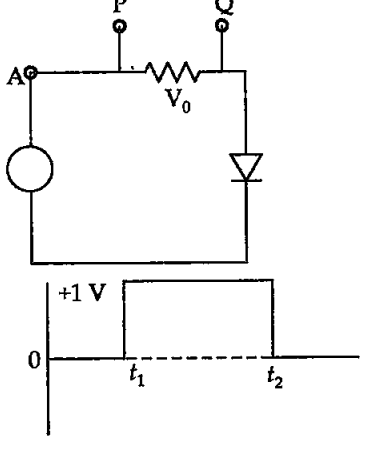
Q14.19. Can the potential barrier across p-n junction be measured by simply connecting a voltmeter across the junction?

Ans. We cannot measure the potential barrier across p-n junction by voltmeter, because the resistance across depletion layer is smaller than resistance of voltmeter so current to measure the potential will not flow in voltmeter, and current passes through the junction.

Q14.20. Draw the output waveform across the resistor in the given figure.



Input waveform at A



Ans. In given circuit waveform is connected at A and waveform obtained across resistance diode conducts when diode is in forward biased so output will be only when input is +1V is between t_1 to t_2. So output waveform will be only t_1 to t_2 which, is in given figure.

Q14.21. The amplifiers X, Y and Z are connected in series. If the voltage gains of X, Y and Z are 10, 20, 30 respectively and input signal is 1 mV peak value, then what is the output signal voltage (peak value)

(*i*) If DC supply voltage is 10 V?

(*ii*) If DC supply voltage is 5 V?

Main concept used: Voltage gain $= \dfrac{\text{Output voltage}}{\text{Input Voltage}}$

Ans. $A_{V_x} = 10$, $A_{V_y} = 20$ and $A_{Vz} = 30$

Signal $A_{V_i} = 1\,\text{mV} = 10^{-3}\,\text{V}$

$$A_V = \frac{V_0}{V_i}$$

$$A_{V_x} \times A_{V_y} \times A_{V_z} = \frac{V_0}{V_i}$$

$$V_0 = V_i \times A_{V_x} \times A_{V_y} \times A_{V_z} = 10^{-3} \times 10 \times 20 \times 30$$

$$= 6\text{V (output signal)}$$

(*i*) If DC supply voltage is 10 V and output voltage 6 V as the theoretical gain and practical gains are equal so output will be 6 V.

(*ii*) When DC supply voltage is 5 V or $V_{ce} = 5$ V then output peak cannot exceed by 5 V. So output will be 5 V.

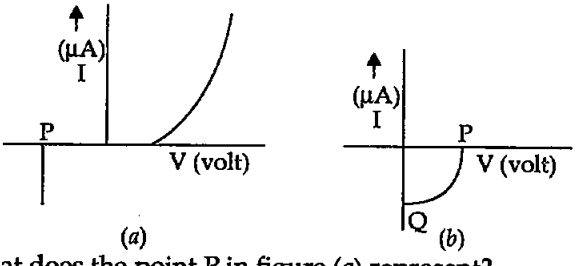
Q14.22. In a CE transistor amplifier, there is a current and voltage gain associated with the circuit. In other words there is a power gain. Considering power a measure of energy, does the circuit violate conservation of energy?

Ans. In CE transistor amplifier the DC supply is connected to give energy to signal. Due to this fact there is a large power gain in CE configuration amplifier.

So energy of output signal is equal to the sum of energy of signal (low) and energy supplied by DC source in output CE circuit (V_{ce}).

SHORT ANSWER TYPE QUESTIONS

Q14.23. (*i*) Name the type of a diode whose characteristics are shown in figures (a) and (b) here



(*ii*) What does the point P in figure (*a*) represent?

(*iii*) What does the points P and Q in figure (*b*) represent?

Ans. (*i*) Diode in figure (a) is Zener diode and figure (*b*) shows solar cell.

(*ii*) Zener breakdown voltage is represented in figure (*a*).

(*iii*) In figure (*b*), Q represents zero voltage and negative current. It means that light energy falling on solar cell with at least minimum threshold frequency gives the current in opposite direction to that due to a battery connected to solar cell. But for point P the battery is short-circuited and hence represents the short-circuited current.

In figure (*b*), Point P represents some positive voltage on solar cell with zero current through solar cell.

So there is a battery connected to a solar cell which gives rise to the equal and opposite current to that in solar cell by virtue of light falling on it.

As current is zero for point P, hence we say P represents open circuit voltage.

Q14.24. Three photodiodes D_1, D_2 and D_3 are made of semiconductors having band gaps of 2.5 eV, 2 eV and 3 eV respectively. Which one will be able to detect light of wavelength 6000 Å?

Ans. $\lambda = 6000\ \text{Å} = 6000 \times 10^{-10}\ \text{m}$

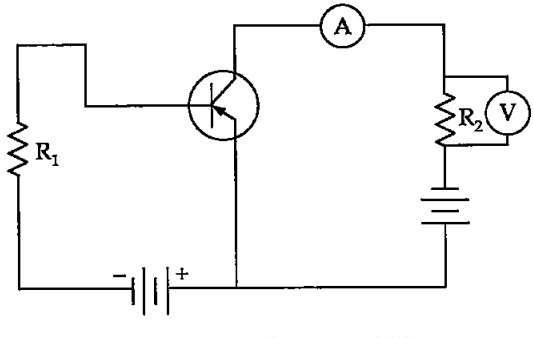
$$E = \frac{hc}{\lambda} = \frac{6.62 \times 10^{-34} \times 3 \times 10^{8}}{6000 \times 10^{-10} \times 1.6 \times 10^{-19}}\ \text{eV}$$

$$= \frac{6.62 \times 3 \times 10^{-34+8+10+19}}{6 \times 1.6 \times 10^{3}}\ \text{eV} = \frac{3.31 \times 10^{-34+37}}{1.60 \times 10^{3}}\ \text{eV}$$

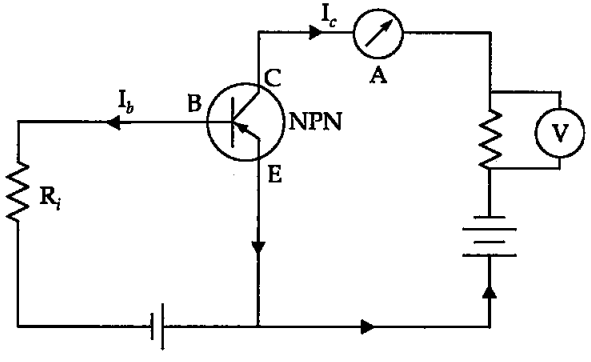
$$= \frac{331}{160} \times \frac{10^{3}}{10^{3}}\ \text{eV} = 2.06\ \text{eV}$$

The incident radiation is detected by the photodiode D_2 has band gap or knee voltage 2 eV only which is less than incident radiation of 2.06 eV.

Q14.25. If the resistance R_1 is increased (see figure) how will the readings of the ammeter and voltmeter change?



Ans. Consider the figure given below to find out the change in reading of output E-C circuit



$$I_B = \frac{V_{BB} - V_{BE}}{R_i}$$

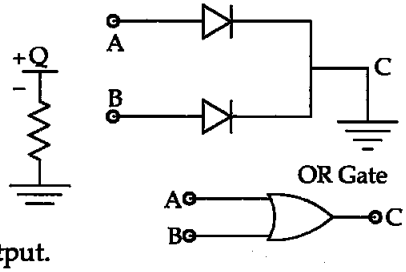
As R_i increases the P.D. across R_i also increases so potential across BE decreases so the Ic will also decrease in turn reading of ammeter and voltmeter will decrease because $Ic = \beta I_B$.

Q14.26. Two car garages have a common gate which needs to open automatically when a car enters either of the garages or cars enter both. Device a circuit that resembles this situation using diodes for this situation.

Ans. When a car enters the gate, any one or both are open.

The device is shown in figure.

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1



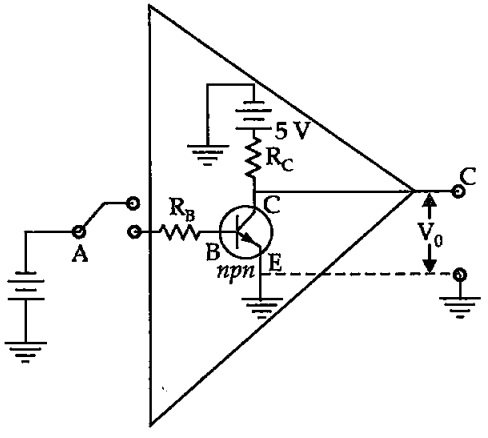
So OR gate gives the desired output.

Q14.27. How would you set up a circuit to obtain NOT gate using a transistor?

Ans. The NOT gate is a device which has only one input and one output *i.e.*, $\bar{A} = Y$ means, Y equals to NOT A. Thus,

A	$Y = \bar{A}$
0	1
1	0

Here the base B of the transistor is connected to the input A through the input resistance R_B and the emitter is earthed. The collector is connected to 5 V battery. The output Y is the voltage at C w.r.t. earth.

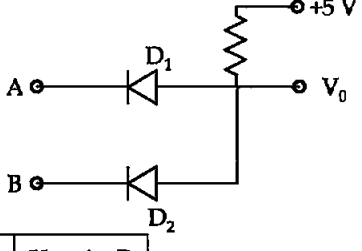


The resistance R_B and R_C are so chosen that if emitter-base junction is unbiased, the transistor is in cut-off region and if emitter-base junction is in forward bias by 5 V input at A, the transistor is in saturation state.

Q14.28. Explain why elemental semiconductor cannot be used to make visible LEDs.

Ans. In elemental conductor, the band gap is such that the **emissions are in infrared region** and **not in visible region.**

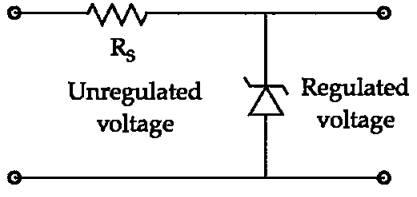
Q14.29. Write the truth table for the circuit shown in figure given alongside. Name the gate that the circuit resembles.



Ans. The circuit resembles AND gate. The boolean expression of this circuit is $V_0 = A.B$ *i.e.*, V_0 equals A AND B. The truth table of this gate is as:

A	B	$V_0 = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

Q14.30. A Zener of power rating 1 W is to be used as a voltage regulator. If Zener has a breakdown of 5 V and it has to regulate voltage which fluctuated between 3 V and 7 V what should be the value of R_S for safe operation (see figure)?



Ans. Given P = 1 Watt

Zener breakdown voltage = 5 V

Minimum voltage $V_{min} = 3$ V

Maximum voltage $V_{max} = 7$ V

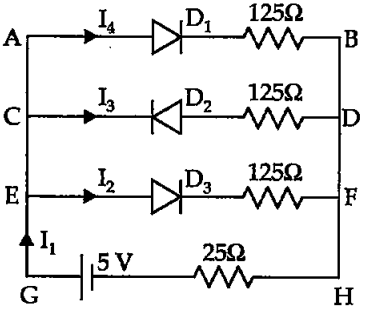
Current = $\boxed{I_{max} = \frac{P}{V_Z}}$

$$I_{Z\,max} = \frac{1\,\text{Watt}}{5} = 0.2\ \text{A}$$

$$\boxed{R_S = \frac{V_{max} - V_{min}}{I_{Z\,max}}} = \frac{7-3}{0.2} = \frac{4}{0.2} = 20\ \Omega$$

LONG ANSWER TYPE QUESTIONS

Q14.31. If each diode in figure has a forward bias resistance of 125 Ω and infinite resistance in reverse bias, what will be the values of the currents I_1, I_2, I_3 and I_4?



Ans. Diode D_1 and D_3 are in forward bias and D_2 is in reverse bias so resistance in arm A B and EF = 125 + 25 = 150 Ω and Resistance in CD is infinite.

$$\frac{1}{R_{24}} = \frac{1}{150} + \frac{1}{150} = \frac{2}{150} = \frac{1}{75}$$

$$R_{24} = 75\ \Omega$$

Total resistance in circuit = R = 75 + 25 = 100 Ω

So $V = IR$

$$5 = I_1\,100$$

$$I_1 = \frac{5}{100} = 0.05\ \text{Amp}$$

$$I_1 = I_2 + I_3 + I_4$$

∴ Resistance R of CD = ∞

so $I_3 = 0$

so $I_1 = I_2 + I_4$

Here resistances are equal

∴ $I_2 = I_4$

or $I_1 = 2I_2$

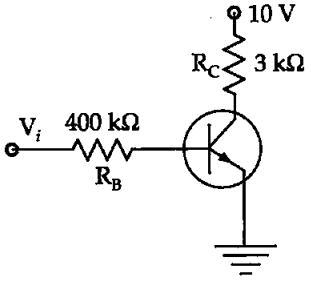
∴ $I_2 = \frac{I_1}{2}$

$$\frac{0.05}{2} = I_2$$

$$I_2 = 0.025$$

$I_1 = 0.05$ Amp, $I_2 = 0.025$ Amp, $I_4 = 0.025$ Amp and $I_3 = 0$ Amp.

Q14.32. In the circuit shown in figure, when the input voltage of the base resistance is 10 V, V_{BE} is zero and V_{CE} is also zero. Find the values of I_B, I_c and β.



Ans. Voltage across $R_B = 10V$

$$V_B = R_B I_B$$

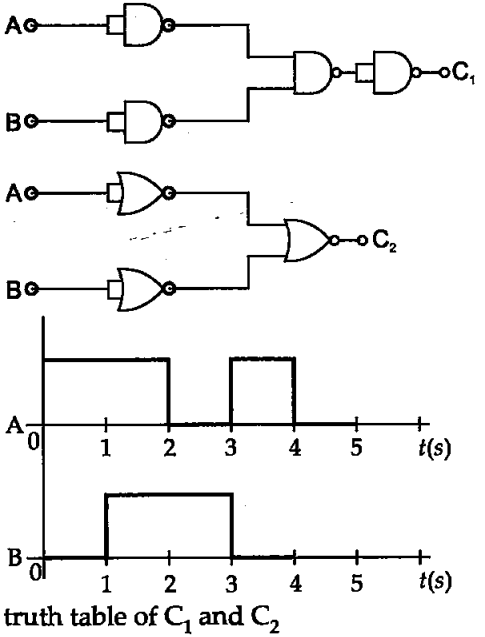
$$I_B = \frac{V_B \text{ (Voltage across } R_B)}{R_B}$$

$$= \frac{10}{400 \times 1000} A = 2.5 \times 10^{-5} A = 25 \times 10^{-6} A$$

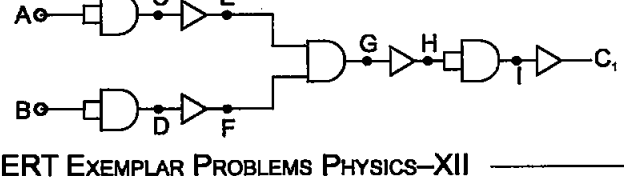
$$I_C = \frac{V_C \text{(Voltage across } R_C)}{R_C} = \frac{10}{3 \times 1000} = 3.3 \times 10^{-3} A$$

$$\text{Current gain } (\beta) = \frac{I_C}{I_B} = \frac{3.3 \times 10^{-3}}{25 \times 10^{-6}} = 133$$

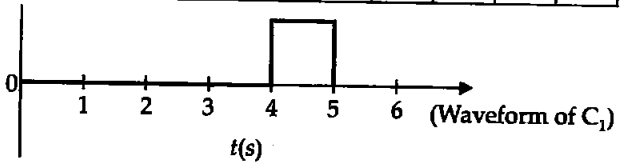
Q14.33. Draw the output signals C_1 and C_2 in the given combination of gates.

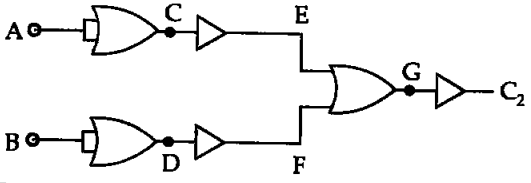


Ans. To draw the truth table of C_1 and C_2

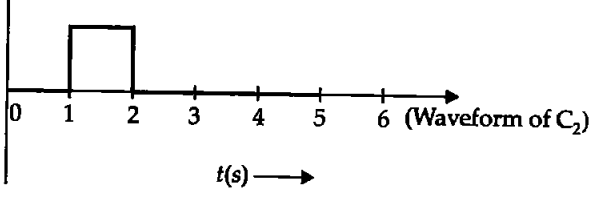


time/sec	A	B	C	D	E	F	G	H	I	C_1
0–1	1	0	1	0	0	1	0	1	1	0
1–2	1	1	1	1	0	0	0	1	1	0
2–3	0	1	0	1	1	0	0	1	1	0
3–4	1	0	1	0	0	1	0	1	1	0
4–5	0	0	0	0	1	1	1	0	0	1

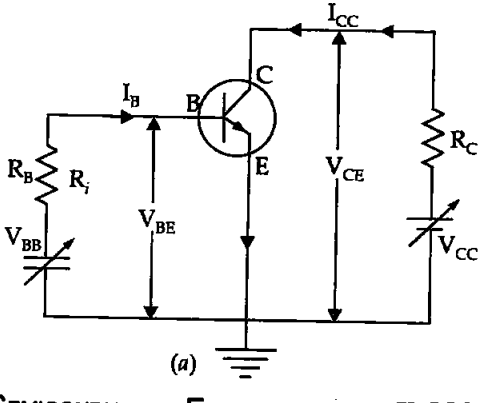


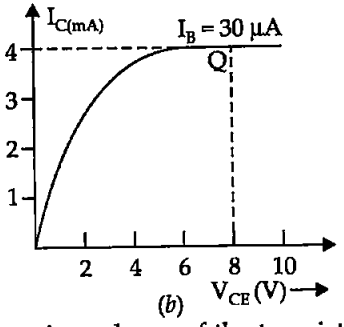


time/sec	A	B	C	D	E	F	G	C_2
0–1	1	0	1	0	0	1	1	0
1–2	1	1	1	1	0	0	0	1
2–3	0	1	0	1	1	0	1	0
3–4	1	0	1	0	0	1	1	0
4–5	0	0	0	0	1	1	1	0



Q14.34. Consider the circuit arrangement shown in figure (*a*) for studying input and output characteristics of *n-p-n* transistor in CE configuration. Select the values of R_B and R_C for a transistor whose V_{BE} = 0.7 Volt, so that the transistor is operating at a point Q as shown in characteristics [figure (*b*)].





(b)

Given that the input impedance of the transistor is very small and $V_{CC} = V_{BB} = 16$ V, also find the voltage gain and power gain of circuit making appropriate assumptions.

Ans. For output characteristics at point Q

$V_{CE} = 8$ V, $I_B = 30\ \mu A$, $I_C = 4$ mA, $V_{BE} = 0.7$ V

Applying Kirchhoff's law in collector-emitter loop

$$V_{CC} = V_{CE} + R_C I_C$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{16-8}{4\times10^{-3}} = \frac{8}{4}\times10^3 = 2000\ \Omega$$

$$R_C = 2000\ \Omega$$

Now applying Kirchhoff's loop law in base-emitter circuit,

$$V_{BB} = I_B R_B + V_{BE}$$

$$R_B = \frac{V_{BB} - V_{BE}}{I_B} = \frac{16-0.7}{30\times10^{-6}} = \frac{15.3\times10^{-6}}{30} = 530\ k\Omega$$

Voltage gain = $A_V = -\beta\frac{R_C}{R_B}$ and $\beta = \frac{I_C}{I_B}$

$$\beta = \frac{4\times10^{-3}}{30\times10^{-6}} = \frac{40}{30}\times10^3 = \frac{4000}{30} = \frac{400}{3}$$

Average Voltage A_V

$$A_V = -\beta\frac{R_C}{R_B}$$

(–) sign shows change in phase angle of output is 180° by input voltage.

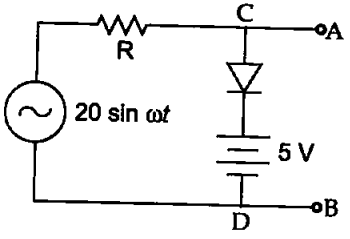
$$A_V = \frac{+400}{3}\times\frac{2000}{530,000} = \frac{80}{15.6} = 0.52$$

Power gain = I.V

Power gain = $\beta \times A_V = 0.52 \times \frac{400}{3}$

Power gain = $\frac{208}{3} = 69.33$ or $P_{gain} = \mathbf{69.33}$

Q14.35. Assuming the ideal diode, draw the output waveform for the circuit given in figure. Explain the waveform.



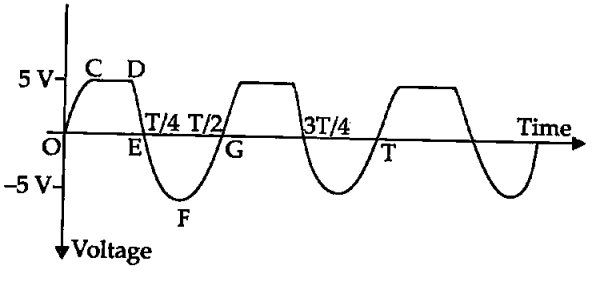
Main concept used: When a diode is in forward bias its resistance is zero and when it is in reverse bias its resistance is infinite.

Ans. When signal 20 sin ωt gives input voltage less than 5 volt (because after 5V diode will get positive voltage at its P-junction) then diode will be in reverse bias so resistance of diode remain infinity so input signal will not pass through diode and battery path so output across A and B will increase from 0 – 5 V (graph OC).

Now when the input voltage 20 sin ωt increase beyond 5 V then path of diode and 5 V battery will offer very low resistance, so the current passes through diode and battery and output (across A and B) remain 5V (graph CD).

Now when the voltage decreases the diode will be in reverse bias and output will again fall from 5 V to 0 V as input changes (graph DE). When input voltage becomes negative (there is opposite of 5 V battery in p-n junction input voltage becomes more than 5 V now) the diode is in reversed bias it will not conduct current through CD, and in output across AB will get same as input AC *i.e.* for negative cycle diode offer infinite resistance as compared to R in series graph E, F, G.

Same repetition of input and output continues—graph showing the output waveform.



Q14.36. Suppose a *n*-type wafer is created by doping Si crystal having 5×10^{28} atoms/m^3 with one ppm concentration of As. On the surface 200 ppm Boron is added to create P region in this wafer. Considering $n_i = 1.5 \times 10^{16}$ m^{-3} (*i*) Calculate the densities of charge carriers in the *n* and *p* regions. (*ii*) Comment which charge carriers would contribute largely for reverse saturation current when diode is reverse biased.

Ans. When As (pentavalent) is added to Si the n-type wafer is created. So the number of majority carriers in n-type wafer,

$$n_e = (N_D \text{ and } D_{Si}) = \frac{1}{10^6} \times 5 \times 10^{28} = 5 \times 10^{22} \text{ /m}^3$$

For number of minority carriers n_h

$$n_e \cdot n_h = n_i^2$$

$$n_h = \frac{n_i^2}{n_e} = \frac{1.5 \times 10^{16} \times 1.5 \times 10^{16}}{5 \times 10^{22}} \qquad (n_i = 1.5 \times 10^{16}/\text{m}^3) \text{ (Given)}$$

$$= 0.3 \times 1.5 \times 10^{32-22} = 0.45 \times 10^{+10} \text{ per m}^3$$

When Boron (Trivalent) is implanted in Si crystal, p-type wafer is formed with number of holes,

$$n_h = (N_D \times n \text{ of Si})$$

$$= \frac{200}{10^6} \times 5 \times 10^{28} = 1000 \times 10^{28-6}$$

$$n_h = 1 \times 10^{25} \text{ per m}^3$$

Minority carrier in p-type wafer

$$n_e \cdot n_h = n_i^2$$

$$n_e = \frac{n_i^2}{n_h} = \frac{1.5 \times 10^{16} \times 1.5 \times 10^{16}}{10^{25}} = 2.25 \times 10^{32-25}$$

$$= 2.25 \times 10^7 \text{ electrons per m}^3$$

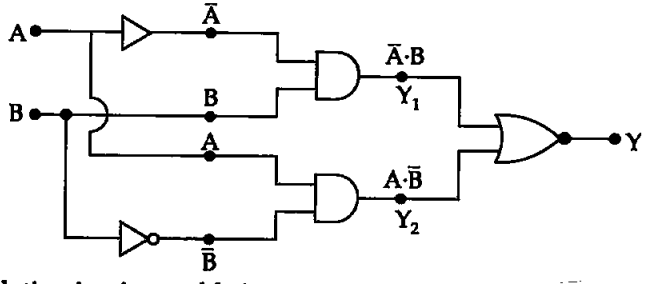
When reversed bias is applied on p-n junction then the minority charge carrier moves toward depletion layer *i.e.*, holes n_h = (0.45×10^{10} per m^3) from n side and $n_e = 2.25 \times 10^7/\text{m}^3$ from p side moves towards junction and make the depletion layer thicker.

Q14.37. An X-OR gate has following truth table. It is represented by following logic relation $Y = \bar{A} \cdot B + A \cdot \bar{B}$. Build this gate using AND, OR and NOT gates.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Ans. In given logic relation $Y = \bar{A}B + A\bar{B} = Y_1 Y_2$

Y	$A.\bar{B}$	$\bar{B}$	A	B	Y	$\bar{A}$	$\bar{A}.B$
0	0	1	0	0	0	1	0
1	0	0	0	1	1	1	1
1	1	1	1	0	1	0	0
0	0	0	1	1	0	0	0



logic relation in given table is

$$Y = \bar{A} \cdot B + A \cdot \bar{B}$$
$$= Y_1 + Y_2$$

$Y_1 = \bar{A} \cdot B$ and $Y_2 = A \cdot \bar{B}$

Y_1 can be obtained by $\bar{A}$ through NOT and B direct to AND gate.

So, $Y_1 = \bar{A} \cdot B$.

Y_2 can be obtained by $\bar{B}$ through NOT and A direct to AND gate.

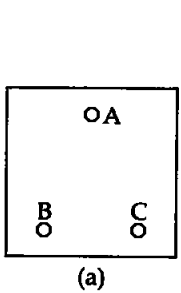
So, $Y_2 = A \cdot \bar{B}$.

Now Y_1 and Y_2 are feed into the two terminals of OR gate to get

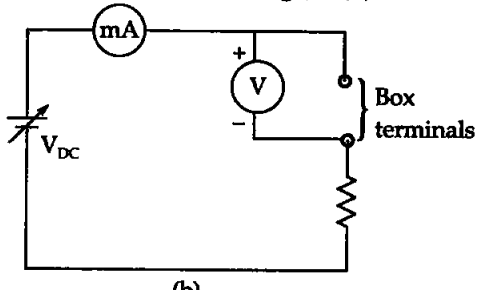
$$Y = Y_1 + Y_2 \quad \text{or} \quad Y = \bar{A}B + A\bar{B}$$

Q14.38. Consider a box with three terminals on the top of it as shown in figure (a). Three components namely, two germanium diodes and one resistor are connected across these three terminals in some arrangement.

A student performs an experiment in which any two of these three terminals are connected in the circuit shown in figure (b).



(a)



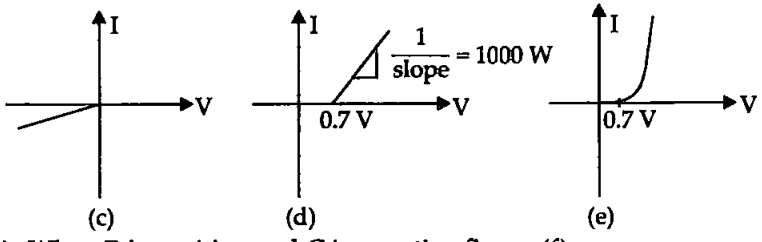
(b)

The student obtains graphs of current-voltage characteristics for unknown combination of the components between the two terminals connected in the circuit. The graphs are:

(*i*) When A is positive and B is negative figure (c)

(*ii*) When A is negative and B is positive figure (d)

(*iii*) When B is negative and C is positive figure (e)

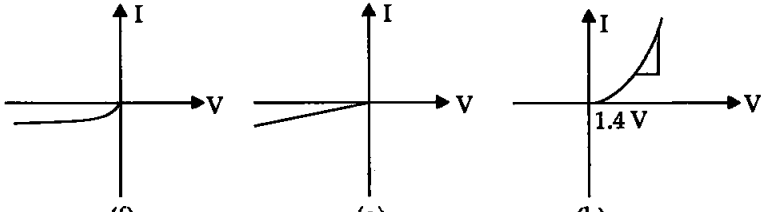


(c) (d) (e)

(*iv*) When B is positive and C is negative figure (f).

(*v*) When A is positive and C is negative figure (g).

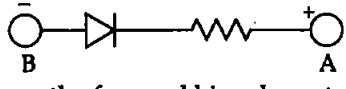
(*vi*) When A is negative and C is positive figure (h).



(f) (g) (h)

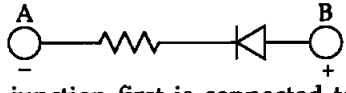
From these graphs of current-voltage characteristics shown in Figure (*c*) to (*h*), determine the arrangement of components between A, B and C.

Ans. (*i*) Figure (*c*) shows the reverse bias characteristics of *p-n* junction. It is possible when *p-n* junction first is in a series combination with *p* side of diode towards B and *n* side towards A resistance. Its resistance is linear or ohmic resistance.



(*ii*) Figure (*d*) shows the forward bias characteristics of a transistor where 0.7 V is the knee voltage of a *p-n* junction first

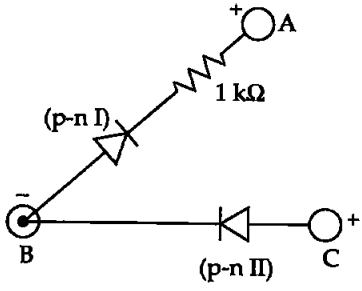
$$\frac{1}{\text{slope}} \Rightarrow \frac{1}{V/I} = V\left(\frac{1}{1000}\right)\Omega$$



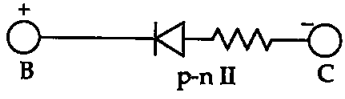
p side of *p-n* junction first is connected to B and *n* side to A terminal. Resistance is in series with diode.

(*iii*) Figure (*e*) also shows the forward bias characteristics of *p-n* junction second having non ohmic as graph is not straight line. It also has knee voltage 0.7 V.

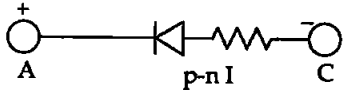
Here *p* side of *p-n* junction is connected to C and n side with B terminal as shown in figure.



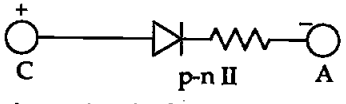
(*iv*) In figure (*f*) graph shows reverse bias characteristics of *p-n* junction II. *n* side with B and p side with C along with a resistance in series.



(*v*) Figure (*g*) shows the reverse bias characteristics of *p-n* junction I.



(*vi*) Figure (*h*) shows forward biased characteristics of *p-n* junction II.



Q14.39. For the transistor circuit shown in figure evaluate V_E, R_B, R_E given that

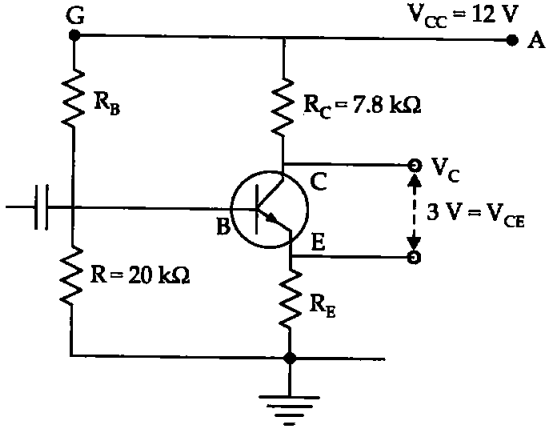
$I_C = 1\text{mA}$

$V_{CE} = 3\text{V}$

$V_{BE} = 0.5\text{V}$

$V_{CC} = 12\text{ V}$

$\beta = 100$



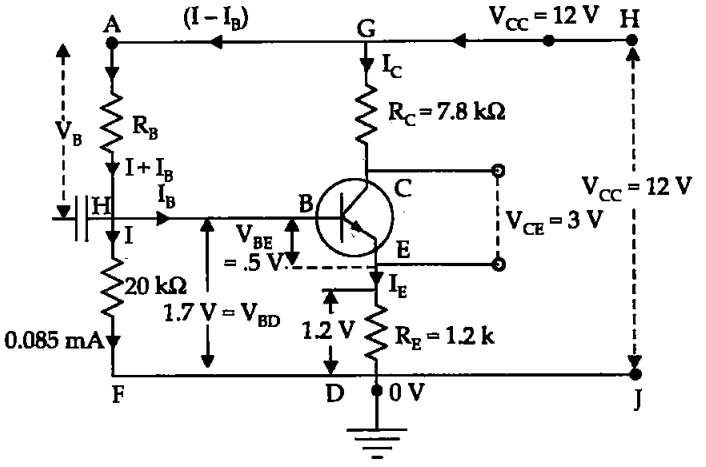
Ans. $I_C = I_B + I_E$

$\because\ I_B \lll I_C$

$\therefore\ I_C = I_E$

$I_C = 1\text{ mA}$ [Given]

$\therefore\ I_E = I_C = 10^{-3}\text{ A}$



$\therefore$ $I_C = I_E = 1$ mA

By Kirchhoff's loop law, in loop DGHJ

$$I_C R_C + I_E R_E + V_{CE} = V_{CC}$$

$$I_C(R_C + R_E) + V_{CE} = 12$$

$$(R_C + R_E)\, 1 \times 10^{-3} + 3 = 12$$

$$R_C + R_E = \frac{9}{10^{-3}}$$

$$7.8 \times 10^3 + R_E = 9000$$

$$R_E = 9000 - 7800 = 1200\ \Omega = 1.2\ k\Omega$$

$$V_E = I_E \times R_E = I_C \times R_E$$

$$= 10^{-3} \times 1200 = 1.2\ V$$

$$V_{BD} = V_E + V_{BE} = 1.2 + 0.5V = 1.7 \text{ volt}$$

$$V_{BE} = 0.5\ V, \text{ and } V_{BE} = 1.2\ V$$

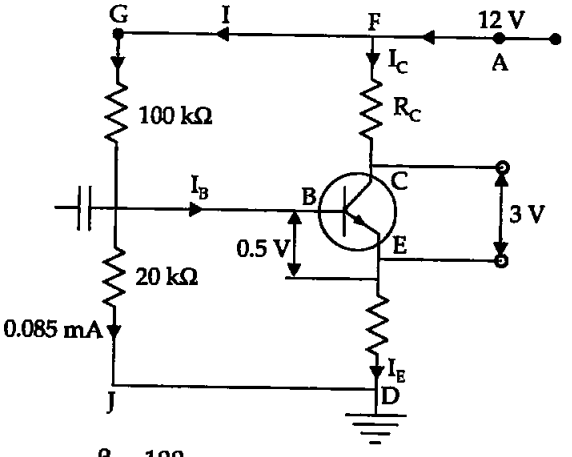
$$I = \frac{V_B}{20000} = \frac{1.7}{20000}\ A = 0.085\ mA$$

$$R_B = \frac{V_{BD}}{(I + I_B)} = \frac{V_{CC} - V_{BD}}{\left[I + \left(\frac{I_C}{\beta}\right)\right]} \qquad \left(\because I_B = \frac{I_C}{\beta}\right)$$

$$R_B = \frac{12 - 1.7}{\left[0.085 + \frac{1}{100}\right] \times 10^{-3}} = \frac{10.3 \times 10^3}{[0.085 + 0.01]} = \frac{10.3 \times 10^3}{0.095}$$

$$= 108 \times 10^3\ \Omega = 108\ k\Omega$$

Q14.40. In the circuit shown in figure find the value of R_C



$\beta = 100$

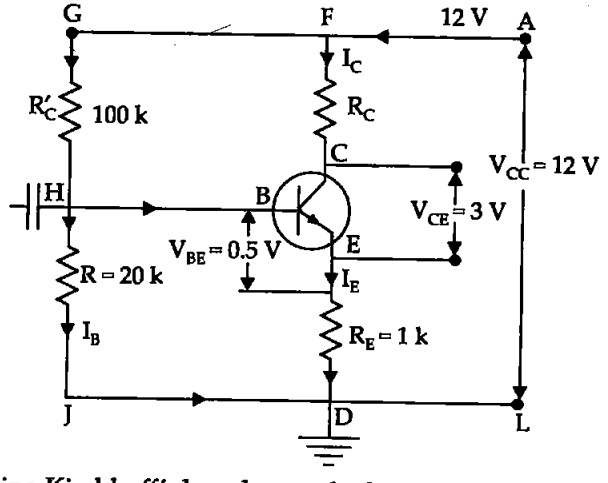
$V_{BE} = 0.5\ V$

$V_{CE} = 3\ V$

Ans. From figure applying Kirchhoff's junction rule at transistor

$$I_e = I_C + I_B \qquad ...(i)$$

$$I_C = \beta I_B \qquad ...(ii)$$



Applying Kirchhoff's loop law to the loop AFCEDLA

$$I_C R_C + V_{CE} + V_E = V_{JA}$$

$$I_C R_C + 3 + I_E R_E = 12\ V \qquad ...(i)$$

$$I_C = I_B + I_E$$

$$I_B <<< I_C$$

$$I_E \cong I_C = \beta I_B \qquad \left(\beta = \frac{I_C}{I_B},\ I_C = I_E\right)$$

From (*i*) $$I_C R_C + I_C R_E = 12 - 3$$

$$R_C \beta I_B + \beta I_B R_E = 9$$

$$\beta I_B (R_C + R_E) = 9 \qquad ...(ii)$$

Applying Kirchhoff's loop law to the loop JHBEDJ

$$RI_B + V_{BE} + R_E I_E = V_{CC}$$

$$I_B R_B + R_E I_E = V_{CC} - V_{BE}$$

$$I_B R + \beta I_B R_E = V_{CC} - V_{BE}$$

$$I_B (R + R_E \beta) = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R + R_E \beta}$$

$$= \frac{12 - 0.5}{(20 + 1 \times 100)\text{K}} = \frac{11.5}{120 \times 10^3}$$

$$I_B = 0.096 \text{ mA}$$

From eqn. (*ii*),

$$R_C + R_E = \frac{9}{\beta I_B} = \frac{9}{(100 \times 0.096)\text{ mA}}$$

$$R_C + 1000 = \frac{9}{9.6 \times 10^{-3}} = 0.938 \text{ k}\Omega$$

$$R_C + 1000 = 938\ \Omega$$

$$R_C = 938 - 1000$$

$$R_C = 62\ \Omega$$

❑❑❑