14 Semiconductor Electronics: Materials, Devices and Simple Circuits

Lesson at a Glance

• Classification of Metals, Conductors and Semiconductors

On the basis of the relative values of electrical conductivity (σ) or resistivity (ρ), the solids are broadly classified as follows:

(*i*) **Metals:** They possess high conductivity and low resistivity. The resistivity of these materials range from 10^{-2} Ω m to 10^{-8} Ω m and the value of conductivity for such materials lie between 10^{2} to 10^{8} S m^{-1}. For example: Ag, Au, Cu, Al, etc.

(*ii*) **Insulators:** They have very high resistivity and very low conductivity. The value of resistivity for these materials lie between 10^{11} to 10^{19} Ω m while the conductivity range is 10^{-11} to 10^{-19} S m^{-1}. For example: rubber, plastic etc.

(*iii*) **Semiconductors:** They have resistivity and conductivity between metals and insulators. The value of resistivity for semiconductors lie between 10^{-5} to 10^{6} Ω m whereas conductivity lies between 10^{5} to 10^{-6} S m^{-1}.

• Intrinsic Semiconductor

The pure semiconductors in which the electrical conductivity is totally governed by the electrons excited from the valence band to the conduction band and in which no impurity atoms are added to increase their conductivity are called intrinsic semiconductors and their conductivity are called intrinsic conductivity.

From diagram, it is clear that the number of electrons so generated will be equal to the number of holes. Hence, in intrinsic semiconductors,

$$n_e = n_h = n_i$$

• Extrinsic Semiconductors

A semiconductor doped with suitable impurity atoms so as to increase its conductivity is called an extrinsic semiconductor Extrinsic semiconductors are of two types:

(*i*) *n*-type semiconductors

(*ii*) *p*-type semiconductors

(*i*) ***n*-type Semiconductors:** The pentavalent impurity atoms are called donors because they donate electrons to the host crystal and the semiconductor doped with donors is called *n*-type semiconductor. In *n*-type semiconductors, electrons are the majority charge carriers and holes are the minority charge carriers. Thus,

$$n_e \cong n_d >> n_h$$

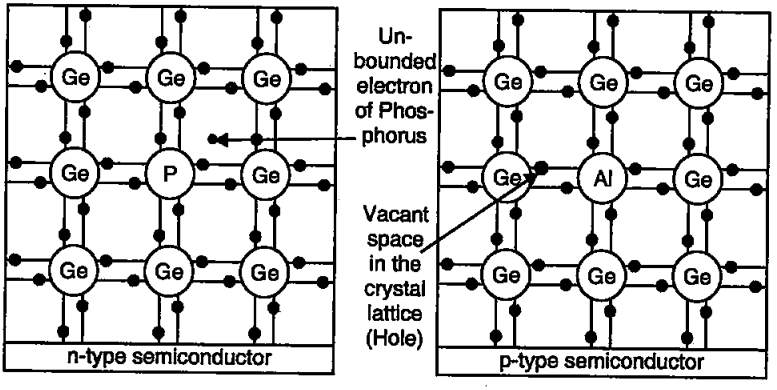


Fig. 14.1

(*ii*) ***p*-type Semiconductors:** The trivalent impurity atoms are called acceptors because they create holes which can accept electrons from the nearby bonds. A semiconductor doped with acceptor type impurities is called a *p*-type semiconductor. In *p*-type semiconductor, holes are the majority carriers and electrons are the minority charge carriers. Thus,

$$N_a \cong n_h >> n_e$$

• *p-n* Junction

It forms the basic unit of a semiconductor device and is referred to as diode. There are many techniques used for creating such junction diodes, as per requirements.

• Zener Diode

Zener diode is a highly doped junction diode having very thin depletion layer.

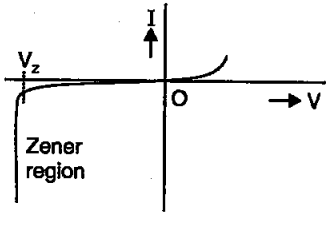
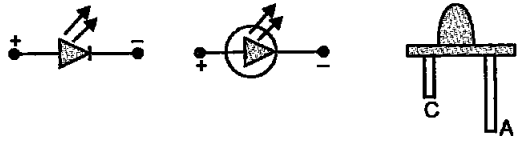


Fig. 14.2

• Light Emitting Diode (LED)

It is a heavily doped *p-n* junction which under forward bias emits spontaneous radiation. When a conduction electron makes a transition to valance band to fill up a hole in *P-N* junction the extra energy may be emitted as a photon lies is the visible range, LED are made of semiconductor materials like gallium arsenide or indium phosphide. These are used in electronic gadgets as indicator lights.

• LED Symbol and Shape



• Solar Cell

In solar cell an electron in the valance band may absorb photon and be promoted to conduction band, leaving a hole behind devices in which light generated electrons and holes are separated by a junction field are called *solar cell or photo voltatic devices.*

• Photodiode

It is a junction diode which operated under reverse bias but less than breakdown voltage.

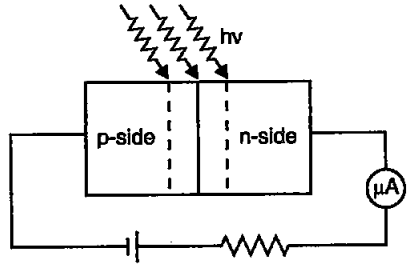


Fig. 14.3

• Transistor

It is a three-layer semiconductor device consisting of two *P*-type and one *N*-type. When *P*-type semiconductor is sandwiched between two *N*-type semiconductor, it is called *N-P-N* transistor. When *N*-type semiconductor is sandwiched between two *P*-type semiconductors, it is called *P-N-P* transistor.

• Logic Gates

It is a digital circuit that follows certain logical relationship between one or more than one input and the output.

These electronic devices work with the binary system of digits *i.e.*, '0' or low level and '1' or high level. They perform some logic operations.

TEXTBOOK QUESTIONS SOLVED

14.1. *In an n-type silicon, which of the following statement is true:*

(a) Electrons are majority carriers and trivalent atoms are the dopants.

(b) Electrons are minority carriers and pentavalent atoms are the dopants.

(c) Holes are minority carriers and pentavalent atoms are the dopants.

(d) Holes are majority carriers and trivalent atoms are the dopants.

Sol. *n*-type is obtained by doping the *Ge* or *Si* with pentavalent atoms. In *n*-type semiconductor, electrons are majority carriers and holes are minority carriers, hence answer (*c*) is true.

14.2. *Which of the statements given in Question 14.1 is true for p-type semiconductors?*

Sol. *p*-type semiconductor is obtained by doping *Ge* or *Si* with trivalent atoms. In *p*-type semiconductor holes are majority carriers and electrons are minority carriers. Hence (*d*) is correct.

14.3. *Carbon, silicon and germanium have four valence electrons each. These are characterised by valence and conduction bands separated by energy band gap respectively equal to* $(E_g)_C$, $(E_g)_{Si}$ *and* $(E_g)_{Ge}$. *Which of the following statements is true?*

(a) $(E_g)_{Si} < (E_g)_{Ge} < (E_g)_C$ *(b)* $(E_g)_C < (E_g)_{Ge} > (E_g)_{Si}$

(c) $(E_g)_C > (E_g)_{Si} > (E_g)_{Ge}$ *(d)* $(E_g)_C = (E_g)_{Si} = (E_g)_{Ge}$

Sol. (*c*) is correct.

As the energy band gap is maximum for carbon, less for silicon and least for germanium out of the given three elements.

14.4. *In an unbiased p-n junction, holes diffuse from the p-region to n-region because*

(a) free electrons in the n-region attract them.

(b) they move across the junction by the potential difference.

(c) hole concentration in p-region is more as compared to n-region.

(d) all the above.

Sol. (*c*) is correct.

As in an unbiased *p-n* junction, hole concentration in *p*-region is more than in *n*-region and due to difference in concentration they diffuse from *p*-region to *n*-region.

14.5. *When a forward bias is applied to a p-n junction, it*

(a) raises the potential barrier.

(b) reduces the majority carrier current to zero.

(c) lowers the potential barrier.

(d) none of the above.

Sol. When a forward bias is applied across the *p-n* junction, the applied voltage opposes the barrier voltage. Due to it, the potential barrier across the junction is lowered. Hence answer (*c*) is correct.

14.6. *For transistor action, which of the following statements are correct:*

(a) Base, emitter and collector regions should have similar size and doping concentrations.

(b) The base region must be very thin and lightly doped.

(c) The emitter junction is forward biased and collector junction is reverse biased.

(d) Both the emitter junction as well as the collector junction are forward biased.

Sol. Statements (*b*) and (*c*) are true.

For a transistor, $\beta = \frac{I_C}{I_B} \Rightarrow I_B = \frac{I_C}{\beta}$

$$R_i = \frac{V_i}{I_B} = \frac{V_i}{I_C}\beta, \quad i.e., \quad R_i \propto \frac{1}{I_c}.$$

Therefore, R_i depends upon collector current I_C. For a transistor action, the emitted junction is forward biased and collector junction is reverse biased.

14.7. *For a transistor amplifier, the voltage gain*

(a) remains constant for all frequencies.

(b) is high at high and low frequencies and constant in the middle frequency range.

(c) is low at high and low frequencies and constant at mid frequencies.

(d) None of the above.

Sol. (c) is correct.

For a transistor amplifier, the voltage gain is low at high and low frequencies and constant at mid frequencies.

14.8. *In half-wave rectification, what is the output frequency if the input frequency is 50 Hz. What is the output frequency of a full-wave rectifier for the same input frequency.*

Sol. Input frequency for half-wave and full-wave rectifier = 50 Hz.

Input and output waveforms of half-wave and full-wave rectifier are shown in figures (*a*) and (*b*).

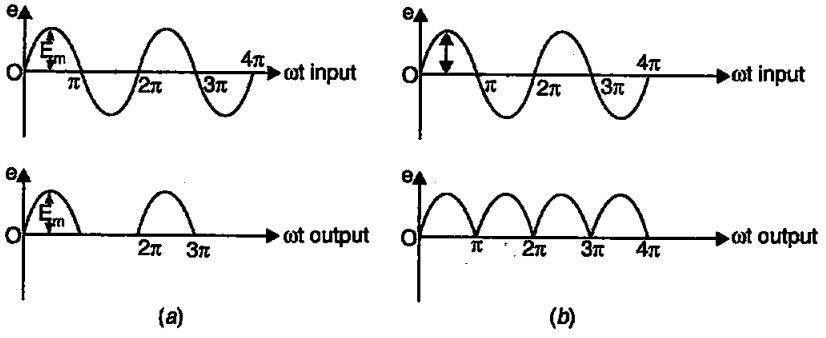


Fig. 14.4

Half-wave rectifier conducts once during a cycle and full-wave rectifier does so twice. Therefore, if input frequency is 50 Hz, output frequency for half-wave and full-wave rectifier are 50 and 100 Hz respectively.

14.9. *For a common emitter-transistor, amplifier, the audio signal voltage across the collector resistance of 2 kΩ is 2 V. Suppose the current amplification factor of the transistor is 100, find the input signal voltage and base current, if the base resistance is 1 kΩ.*

Sol. Here, $R_0 = 2000\ \Omega$; $V_0 = 2$ V,

$\beta_{ac} = 100$; $V_i = ?$

$I_b = ?$ $R_i = 1000\ \Omega$

As, $$A_V = \frac{V_0}{V_i} = \beta_{ac} \frac{R_0}{R_i}$$

or, $$V_i = \frac{V_0}{\beta_{ac} \cdot (R_0/R_i)} = \frac{2}{100\,(2000/1000)} = 0.01 \text{ V}$$

$$I_b = \frac{V_i}{R_i} = \frac{0.01\,V}{1000\,\Omega} = 10\ \mu\text{A}$$

14.10. *Two amplifiers are connected one after the other in series (cascaded). The first amplifier has a voltage gain of 10 and the second has a voltage gain of 20. If the input signal is 0.01 V, calculate the output a.c. signal.*

Sol. Total voltage gain $A_V = \frac{\Delta V_0}{\Delta V_i} = A_{V_1} \times A_{V_2}$

or, $$\Delta V_0 = \Delta V_i \times A_{V_1} \times A_{V_2}$$
$$= 0.01 \times 10 \times 20 = 2 \text{ V}.$$

14.11. *A p-n photodiode is fabricated from a semiconductor with band gap of 2.8 eV. Can it detect a wavelength of 600 nm?*

Sol. Energy, $$E = \frac{hc}{\lambda} = \frac{6.6 \times 10^{-34} \times 3 \times 10^8}{600 \times 10^{-9} \times 1.6 \times 10^{-19}} \text{ eV}$$

$$= 2.06 \text{ eV} < 2.8 \text{ eV}$$

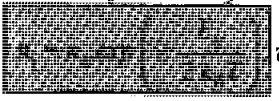
As $E < E_g$, so *p-n* junction cannot detect the radiation of given wavelength.

14.12. *The number of silicon atoms per m^3 is 5×10^{28}. This is doped simultaneously with 5×10^{22} atoms per m^3 of Arsenic and 5×10^{20} per m^3 atoms of Indium. Calculate the number of electrons and holes. Given that $n_i = 1.5 \times 10^{16}\ m^{-3}$. Is the material n-type or p-type?*

Sol. $$n_e = 5 \times 10^{22} - 5 \times 10^{20}$$
$$= (5 - 0.05) \times 10^{22}$$

$$n_h = \frac{n_i^2}{n_e} = \frac{(1.5 \times 10^{16})^2}{4.95 \times 10^{22}} = 4.54 \times 10^9 \text{ m}^{-3}$$

As $n_e > n_h$, so the material is *n*-type semiconductor.

14.13. *In an intrinsic semiconductor the energy gap E_g is 1.2 eV. Its hole mobility is much smaller than electron mobility and independent of temperature. What is the ratio between conductivity at 600 K and 300 K? Assume that the temperature dependence of intrinsic carrier concentration n_i is given by*  *where n_0 is a constant and $k_B = 8.62 \times 10^{-5}$ eV/K.*

Sol.

$$\frac{n_{i_1}}{n_{i_2}} = \frac{e^{\frac{1.2\,eV}{2 \times k_B \times 600}}}{e^{\frac{1.2\,eV}{2 \times k_B \times 300}}}$$

$$= e^{\frac{1.2\,eV}{2 \times k_B}\left(\frac{1}{300} - \frac{1}{600}\right)}$$

$$= e^{\frac{1.2 \times 1.6 \times 10^{-19}}{2 \times 1.381 \times 10^{-23} \times 600}}$$

or,
$$\frac{n_{i_1}}{n_{i_2}} = e^{11.59} = 1.072 \times 10^5$$

(Let $x = e^{11.59} \Rightarrow \log x = 11.59 \log_e$

$$\Rightarrow \log_{10} x = \frac{11.59}{2.303} = 5.03$$

x = antilog 5.03 = 1.072×10^5).

14.14. *In a p-n junction diode, the current I can be expressed as*  *where I_0 is called the reverse saturation current, V is the voltage across the diode and is positive for forward bias and negative for reverse bias, and I is the current through the diode, k_B is the Boltzmann constant (8.6×10^{-5} eV/K) and T is the absolute temperature. If for a given diode $I_0 = 5 \times 10^{-12}$ A and T = 300 K, then*

(a) What will be the forward current at a forward voltage of 0.6 V?

(b) What will be the increase in the current if the voltage across the diode is increased to 0.7 V ?

(c) What is the dynamic resistance?

(d) What will be the current if reverse bias voltage changes from 1 V to 2 V?

Sol. Here, $I_0 = 5 \times 10^{-12}$ A, $T = 300$ K

$$k_B = 8.6 \times 10^{-5} \text{ eVk}^{-1}$$

$$= 8.6 \times 10^{-5} \times 1.6 \times 10^{-19} \text{ JK}^{-1}$$

(*a*) If $V = 0.6$ V, then $\dfrac{eV}{k_B T}$

$$= \frac{1.6 \times 10^{-19} \times 0.6}{8.6 \times 10^{-5} \times 1.6 \times 10^{-19} \times 300} = 23.26$$

$$I = I_0 \left[\exp\left(\frac{eV}{k_B T} - 1 \right) \right]$$

$$= 5 \times 10^{-12} [e^{23.26} - 1]$$

$$= 5 \times 10^{-12} [1.259 \times 10^{10} - 1]$$

$$= 5 \times 10^{-12} \times 1.259 \times 10^{10} = 0.063 \text{ A}$$

(*b*) If $V = 0.7$ V, then $\dfrac{eV}{k_B T}$

$$= \frac{1.6 \times 10^{-19} \times 0.7}{8.6 \times 10^{-5} \times 1.6 \times 10^{-19} \times 300} = 27.14$$

$$I = I_0 \left[\exp\left(\frac{eV}{k_B T} - 1 \right) \right]$$

$$= 5 \times 10^{-12} [e^{27.14} - 1]$$

$$= 5 \times 10^{-12} [6.07 \times 10^{11} - 1]$$

$$= 5 \times 10^{-12} \times 6.07 \times 10^{11} = 3.035 \text{ A}$$

$\therefore$ Increase in current,

$$\Delta I = (3.035 - 0.063) = 2.972 \text{ A}$$

(*c*) As, $\Delta I = 2.972$ A, $\Delta V = 0.7 - 0.6 = 0.1$ V

$$\text{Dynamic resistance} = \frac{\Delta V}{\Delta I} = \frac{0.1\text{ V}}{2.972\text{ A}} = 0.0336\ \Omega$$

(*d*) For both the voltages, the current I will be almost equal to I_0 showing almost infinite dynamic resistance in the reverse bias.

14.15. *You are given the two circuits as shown in figure. Show that circuit (a) acts as OR gate while the circuit (b) acts as AND gate.*

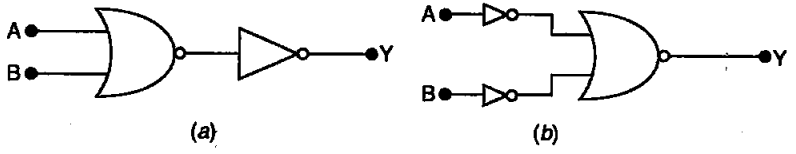


Fig. 14.5

Sol. (*a*) Here in figure (*a*) input A and B is given to NOR gate. So the output of NOR gate is Y'.

A	B	Y'
0	0	1
0	1	0
1	0	0
1	1	0

Now Y' is input for NOT gate. So output Y is represented in form of truth table as shown.

Input Y'	*Output* $Y = Y'$
1	0
0	1
0	1
0	1

Which is same as truth table of OR gate.

(*b*) Here in figure (*b*), input A and B are given to two NOT gates and these inverted input is provided to NOR gate. Its truth table can be represented as

		Output of NOT gates	
A	B	$\overline{A}$	$\overline{B}$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	0	0

Now output of NOT gate is fed as input to NOR gate. So its truth table can be represented as

Input		Output
$\overline{A}$	$\overline{B}$	Y
1	1	0
1	0	0
0	1	0
0	0	1

which represents AND operation.

14.16. *Write the truth table for a NAND gate connected as given in figure.*

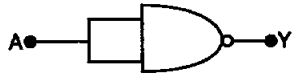


Fig. 14.6

Hence identify the exact logic operation carried out by this circuit.

Sol. The truth table for the circuit:

A	Y
0	1
1	0

This can be represented as $Y = \overline{A}$

The circuit represents the NOT gate.

14.17. *You are given two circuits as shown in figure, which consist of NAND gates. Identify the logic operation carried out by the two circuits.*

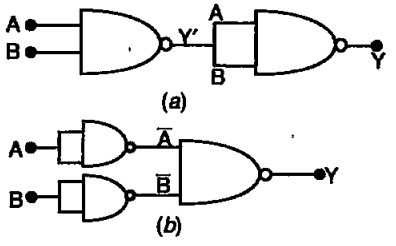


Fig. 14.7

Sol. The truth table for first circuit: (*a*)

A	*B*	*Y'*	*Y*
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

If we remove the intermediate output *Y'*, the overall result stands for the AND gate.

A	*B*	*Y*
0	0	0
0	1	0
10	0	0
1	1	1

Hence, the circuit is an equivalent of AND gate.

The truth table for second circuit: (*b*)

A	B	$\overline{A}$	$\overline{B}$	Y
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

If we remove the intermediate output $\overline{A}$ and $\overline{B}$, the overall result stands for the OR gate.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

This can be represented as $Y = A + B$

Hence, the circuit is an equivalent of OR gate.

14.18. *Write the truth table for circuit given in figure below consisting of NOR gates and identify the logic operation (OR, AND, NOT), which this circuit is performing.*

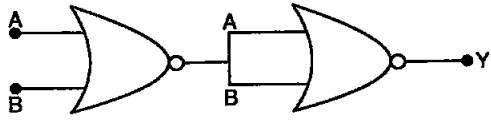


Fig. 14.8

(**Hint:** *A = 0, B = 1 then A and B inputs of second NOR gate will be 0 and hence Y = 1. Similarly work out the values of Y for other combinations of A and B. Compare with the truth table of OR, AND, NOT gates and find the correct one.)*

Sol. In the given figure first portion represents NOR gate, second represents NOT gate. First we calculate output of 1 which acts as input for 2. 2 inverts it and we get final output Y.

A	B	$A+B$	$\overline{A+B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

A	B	$\overline{A+B}$	$Y = \overline{\overline{A+B}}$
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

Which is truth table for OR gate.

14.19. *Write the truth table for the circuits given in figure. Consisting of NOR gates only. Identify the logic operations (OR, AND, NOT) performed by the two circuits.*

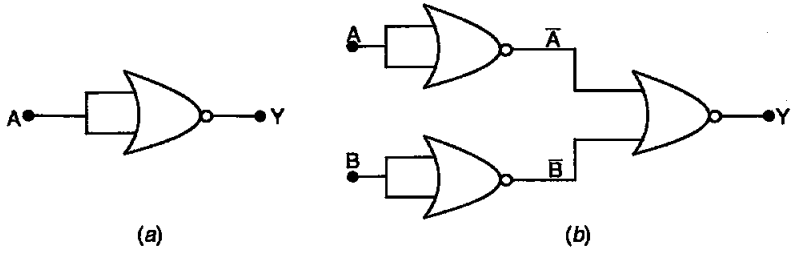


Fig. 14.9

Sol. Figure (*a*) represents NOT gate.

Here when $A = 1, \quad Y = 0$

and when $A = 0, \quad Y = 1$

Figure (*b*) represents two NOT gates whose outputs are given to NOR gate.

Its truth table is

A	B	$\overline{A}$	$\overline{B}$	Y
0	0	1	1	0
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1

Y is truth table of AND gate.

Logic operation performed by figure (*b*) is AND operation.

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